CLAIMS

1. A method for programming programmable elements of a plurality of memory devices, each memory device having at least a first and second programmable element thereon, the method comprising:

programming the first programmable element of a first memory device of the plurality; and

programming the second programmable element of a second memory device of the plurality, the programming of the first and second programmable elements overlapping at least for a period of time.

2. The method of claim 1 wherein the programming of the first and second programmable elements occur substantially concurrently.

3. The method of claim 1 wherein the programming of the first and second programmable elements occur substantially sequentially.

4. The method of claim 1 wherein programming of the first programmable element comprises:

providing bank and fuse addresses corresponding to the first programmable element;

latching the bank address;

latching the fuse address; and

initiating a programming event in response to latching the fuse address to program the first programmable element.

5. The method of claim 4 wherein providing the fuse address ceases prior to the completion of the programming event.

6. The method of claim 1 wherein programming of the first programmable element comprises:

providing a bank address corresponding to an antifuse bank in which the first programmable element is located;

providing a first load command to latch the bank address;

providing a fuse address corresponding to the first programmable element;

providing a second load command to latch the fuse address; and

initiating a programming event in response to latching the fuse address to program the first programmable element.

7. The method of claim 1 wherein the programmable element comprises an antifuse.

8. The method for programming programmable elements of a plurality of memory devices, comprising:

in a first memory device of the plurality, latching a first address corresponding to a programmable element located at a first location on the memory devices;

initiating a programming event to program the programmable element in the first memory device located at the first location;

in a second memory device of the plurality, latching a second address corresponding to a programmable element located at a second location on the memory devices; and

before the completion of the programming event for the programmable element in the first memory device, initiating a programming event to program the programmable element in the second memory device located at the second location.

9. The method of claim 8 wherein the programming events for the programmable elements in the first and second devices occurs substantially concurrently.

10. The method of claim 8 wherein the programming events for the programmable elements in the first and second devices occurs substantially sequentially.

11. The method of claim 8 wherein latching the first address comprises:

the address latch is a first address latch and providing a first load command to the first memory device to latch the bank address;

providing a fuse address corresponding to the programmable element located at the first location; and

providing a second load command to the first memory device to latch the fuse address.

12. The method of claim 11 wherein providing the fuse address corresponding to the programmable element located at the first location ceases prior to the completion of the programming event for the programmable element in the first memory device.

13. The method of claim 8 wherein the latching of the first address and the second address occur substantially simultaneously.

14. A method for an external tester to program programmable elements of a plurality of memory devices, comprising:

commanding a first of the memory devices to latch a first address corresponding to a programmable element located at a first location on the memory devices;

commanding a second of the memory devices to latch a second address corresponding to a programmable element located at a second location on the memory devices; and

programming the programmable elements of the first and second of the memory devices substantially concurrently.

15. The method of claim 14 wherein the programming of the programmable elements of the first and second of the memory devices is initiated substantially simultaneously.

16. The method of claim 14 wherein the programming of the programmable elements of the first and second of the memory devices is initiated substantially sequentially.

17. The method of claim 14 wherein commanding the first and the second of the memory devices comprises simultaneously providing a load command to the first and second of the memory devices.

18. The method of claim 14 wherein commanding the first and the second of the memory devices comprises sequentially providing a load command to the first and second of the memory devices.

19. The method of claim 14, further comprising providing the first address and the second address to the first and second of the memory devices, respectively, substantially simultaneously.

20. A method for an external tester to program antifuses of a plurality of memory devices, comprising:

providing to a first memory device of the plurality an address corresponding to a programmable element to be programmed in the first memory device;

providing a load command to the first memory device to latch the address;

providing to a second memory device of the plurality an address corresponding to a programmable element to be programmed in the second memory device; and

providing a load command to the second memory device to latch the address.

21. The method of claim 20 wherein providing a load command to the first memory device and providing a load command to the second memory device occur simultaneously.

22. The method of claim 20 wherein providing a load command to the first memory device and providing a load command to the second memory device occur sequentially.

23. The method of claim 20 wherein providing an address to the first memory device and providing an address to the second memory device occur simultaneously.

24. The method of claim 20 wherein providing an address to the first memory device and providing an address to the second memory device occur sequentially.

25. The method of claim 20 wherein providing an address to the first and second memory devices ceases prior to the completion of a antifuse programming event.

26. A memory device having external address terminals and an array of memory with redundant memory to replace memory cells therein in accordance with programmed programmable elements, the memory device comprising:

an address latch for latching an address corresponding to a programmable element to be programmed by a programming event;

logic circuitry coupled to the address latch, the logic circuitry receiving address load commands and providing control signals to the address latch in response thereto to cause the address latch to latch an address applied to the external address terminals as the address corresponding to a programmable element to be programmed; and

programming circuitry coupled to the address latch and at least a portion of the programmable elements, the programming circuitry performing a programming event to program the programmable element corresponding to the latched address.

27. The memory device of claim 26 wherein the array of memory is divided into a plurality of banks of memory and the memory device further comprises a corresponding plurality of address latches.

28. The memory device of claim 26, further comprising external data terminals to which the load commands are applied.

29. The memory device of claim 26 wherein the address latch comprises a bank address latch for latching a bank address corresponding to an antifuse bank in which the programmable element is located and further comprising a fuse address latch for latching a fuse address corresponding to the programmable element.

30. A memory device having external address terminals and an array of memory with redundant memory to replace memory cells therein in accordance with programmed antifuses, the memory device comprising:

a bank address latch for latching a bank address corresponding to an antifuse bank in which an antifuse to be programmed by a programming event is located;

a fuse address latch for latching an antifuse address corresponding to the antifuse to be programmed by the programming event; and

logic circuitry coupled to the bank and fuse address latches, the logic circuitry receiving address load commands and providing control signals to the bank and fuse address latches in response thereto to cause the latches to latch the respective addresses applied to the external address terminals as the address corresponding to the programmable element to be programmed.

31. The memory device of claim 30, further comprising programming circuitry coupled to the bank and fuse address latches, the programming circuitry performing the

programming event to program the antifuse corresponding to the latched bank and fuse addresses.

32. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

external address terminals;

an array of memory with redundant memory to replace memory cells therein in accordance with programmed programmable elements;

an address latch for latching an address corresponding to a programmable element to be programmed by a programming event;

logic circuitry coupled to the address latch, the logic circuitry receiving address load commands and providing control signals to the address latch in response thereto to cause the address latch to latch an address applied to the external address terminals as the address corresponding to a programmable element to be programmed; and

programming circuitry coupled to the address latch and at least a portion of the programmable elements, the programming circuitry performing a programming event to program the programmable element corresponding to the latched address.

33. The computer system of claim 32 wherein the array of memory of the memory device is divided into a plurality of banks of memory and the memory device further comprises a corresponding plurality of address latches.

34. The computer system of claim 32 wherein the memory device further comprises external data terminals to which the load commands are applied.

35. The computer system of claim 32 wherein the address latch of the memory device comprises a bank address latch for latching a bank address corresponding to an antifuse bank in which the programmable element is located and further comprising a fuse address latch for latching a fuse address corresponding to the programmable element.